GaAs FET's Gate Current Behavior and Its Effects on RF Performance and Reliability in SSPA's

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Abstract— **This paper presents a detailed experimental investigation of gate current limitation effects on power GaAs FET's rf performances. This limitation is accomplished entirely by dynamic compensation of the gate bias voltage. Effects of this current limitation on power added efficiency and output power performances have been examined through an extensive experimental investigation using active second-harmonic loading over the entire Smith chart. Comprehensive results are given and enable the determination of the optimal gate resistor value needed in the dc path for gate current limitation. Thermal runaway problem is also considered when selecting the gate resistor. The current limitation mechanism is analyzed in the case where the gate voltage is controlled in a feedback loop for linearization purposes. Measurements performed on a feedback linearized amplifier are presented and show the behavior of the gate current and its effects on intermodulation product levels.**

I. Introduction

IT IS WELL KNOWN that excessive gate current is harmful to the long term reliability of power GaAs FET's [1], [2]. This current is generated when the positive peak of the rf signal at the gate of a FET is high enough to forward bias the gate junction in a pulsed pattern, or when the negative peak is low enough to force a pulsed avalanche current through the gate. The two events may occur alternatively from one half cycle of the rf signal to another. The gate and drain rf voltages and the gate-source static voltage dictate whether the forward (positive) pulsed current or the avalanche (negative) pulsed current will be predominant. A combination of these currents results in a dc current flowing through the gate.

The most widely used technique for limiting the amplitude of this dc gate current is to insert a series resistor in the dc path of the gate bias circuit, isolated from the AC path to avoid its interaction with the rf signal itself (see Fig. 1). This gate compensation resistor, RG, proportionally converts the average gate current into a voltage drop in series with the gate voltage supply, and thus acts as an auto-compensation circuit. Depending on the input rf power, the resultant dc voltage applied to the gate is dynamically adjusted in order to reduce the gate current. This may result in considerable variations in the gate dc voltage. Increasing the value of RG reduces these variations, but at the same time increases the chances to reach thermal runaway conditions when no rf signal is applied. This thermal runaway is due to the positive feedback of the leakage current between the gate and the source. Manufacturers generally recommend specific values for RG for power MESFET's.

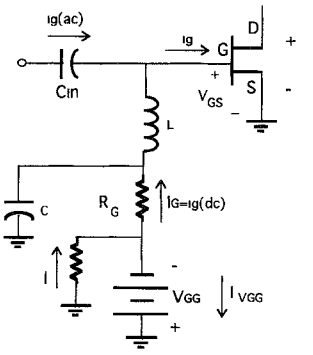

Fig. 1. Equivalent circuit for gate biasing.

The principle of the gate current limitation has been described in the literature [1]. However, its effects on the rf performance of a transistor in terms of power and power added efficiency during characterization or in circuit implementation, and the effects of the output multiharmonic load impedances on the gate current have not been reported in the open literature. Furthermore, there is a lack of papers investigating the typical variations of the gate current as a function of rf power and different gate resistor values. In addition, no experimental or analytical approach to determine the optimal value of the compensation resistor, for a given specific power FET, which offers the best compromise between current limitation and thermal runaway [3] conditions has been reported. Also, there are no published measurement results showing the behaviors of the gate current and the compensation mechanism in linearized amplifiers using feedback control in the gate biasing circuit [4].

This paper presents a comprehensive investigation of the current limitation effects based on an experimental approach along with results obtained for a 3 Watt GaAs FET at 1.7 GHz (FLL351ME from FUJITSU). These results focus on the relationship and the interdependency between average gate current, input rf power level, and the load impedance. Load-pull measurements are presented which, for the first time, show the dependence of the gate current on the output fundamental and second-harmonic load impedances. Measurements

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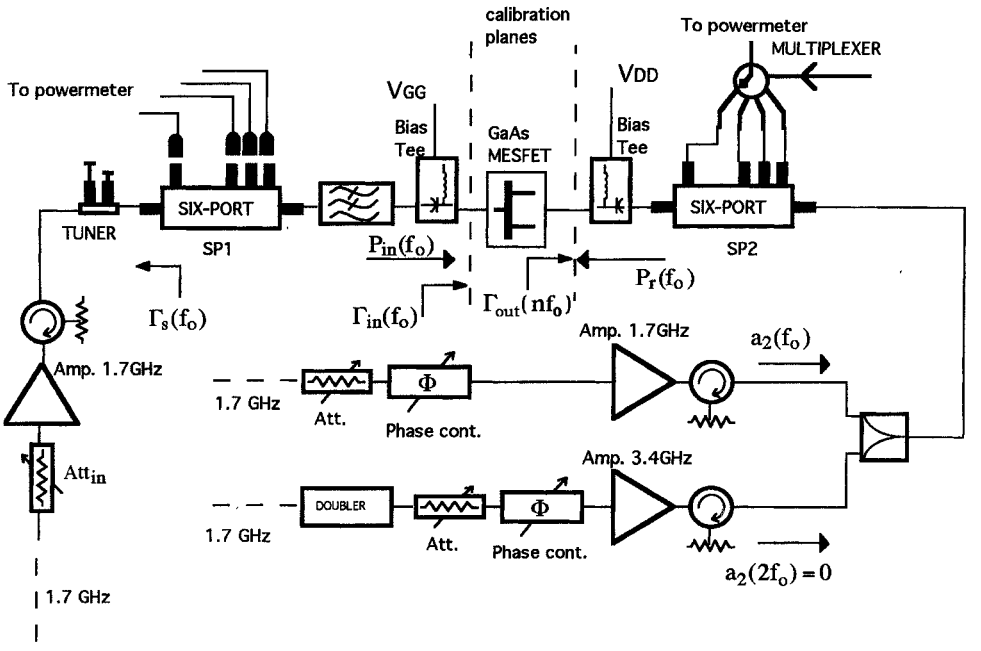


Fig. 2. Multiharmonic active load-pull system.

showing the effects of gate current limitation on output power and power added efficiency in a second-harmonic load-pull environment are also presented for the first time. An experimental approach for the determination of the optimum value of RG that minimizes the gate current without any risk of provoking thermal runaway is discussed. The gate current limitation mechanism within the typical feedback architecture used for amplifier linearization is discussed, and experimental results showing the current behavior as well as its effects on intermodulation product levels are presented.

II. Study of the Gate Current Limitation Effects on Output Power and Power Added Efficiency

An automated multiharmonic active load-pull system similar to those presented in [5] and [6] but operating at a higher power level has been developed for these experiments. Part of this system is illustrated in Fig. 2. The use of active loads allows to vary the reflection coefficient at the fundamental frequency, 1.7 GHz, while the reflection coefficient at the 3.4 GHz harmonic frequency is kept constant, and vice versa. In addition, the use of a six-port reflectometer [7] allows the precise maintenance of a constant absorbed rf power ($P_{\text{in}}(f_0)$) by the FET during measurements. Good precision in the leveling of $P_{\text{in}}(f_0)$ is an essential condition for accurate monitoring of the gate current as a function of the load impedance, since the peak gate-drain and gate-source rf voltages are particularly sensitive to changes in the level of $P_{\text{in}}(f_0)$ in the optimum power region. A second reflectometer is used to measure the output power and the multiharmonic load reflection coefficients $\Gamma_{\text{out}}(nf_0)$ [5].

An FLL351ME power GaAs FET [8] was tested in a class AB operation mode, $I_{\text{DS}} = 12\%\ I_{\text{DSS}}$, for the purpose of finding the optimum power added efficiency and output power conditions, at an output power level condition close to the 1 dB compression point. By maintaining an input power $P_{\text{in}}(f_0)$ constant at 250 mW $\pm$ 5 mW, and a constant reflection coefficient at 3.4 GHz ($\Gamma_{\text{out}}(2f_0) = 0.48\angle -17°$, the passive impedance of the six-port junction), the output power and power added efficiency variations with respect to the load at 1.7 GHz ($\Gamma_{\text{out}}(f_0)$) were simultaneously measured when $R_G = 0\ \Omega$. The results obtained are shown in Fig. 3(a) and (b), respectively. The same measurements were performed using an $R_G = 270\ \Omega$. As will be shown in the next section, this value significantly reduces the gate current variations. The results obtained are presented in Fig. 3(c) and (d). By comparing the results of both experiments we can deduce that the output power and power added efficiency performances are quasi-independent of the value of the resistor needed for current limitation purpose. Only a shift of 7 degrees and a slight decrease (by 3.3%) in the magnitudes of the optimum load conditions are observed (from $\Gamma_{\text{out}}(f_0) = 0.64\angle\ 180°$ to $\Gamma_{\text{out}}(f_0) = 0.62\angle\ 173°$ for power added efficiency).

III. Dependence of Gate Current on the Load Impedance

Load-pull measurements on the average gate current have been performed for the same bias and input power conditions: $I_{\text{DS}} = 12\%\ I_{\text{DSS}}$ and $P_{\text{in}} = 250\ \text{mW} \pm 5\ \text{mW}$. Fig. 4(a) shows the variations of the gate current as a function of $\Gamma_{\text{out}}(f_0)$ with $\Gamma_{\text{out}}(2f_0)$ kept constant at $0.48\ \angle -17°$ and with $R_G = 0\ \Omega$. These results show a very strong dependence of the average gate current on the fundamental load impedance. The extreme values of the gate current were -40 mA (coming out of the gate) and $+10$ mA (entering the gate). These values fall far outside the range recommended by the manufacturer (-2 mA to $+4$ mA). Furthermore, a comparison based on the results of

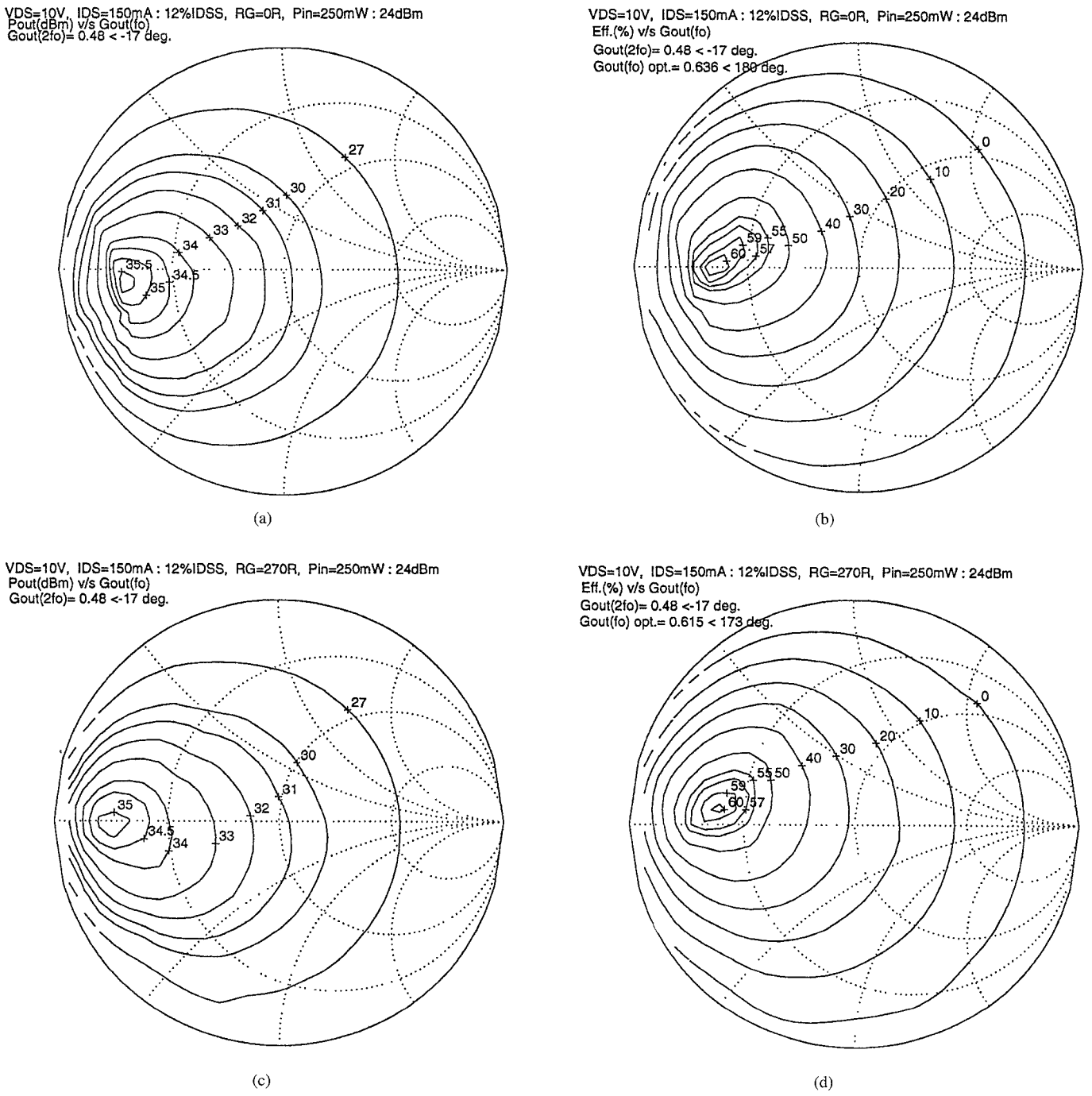
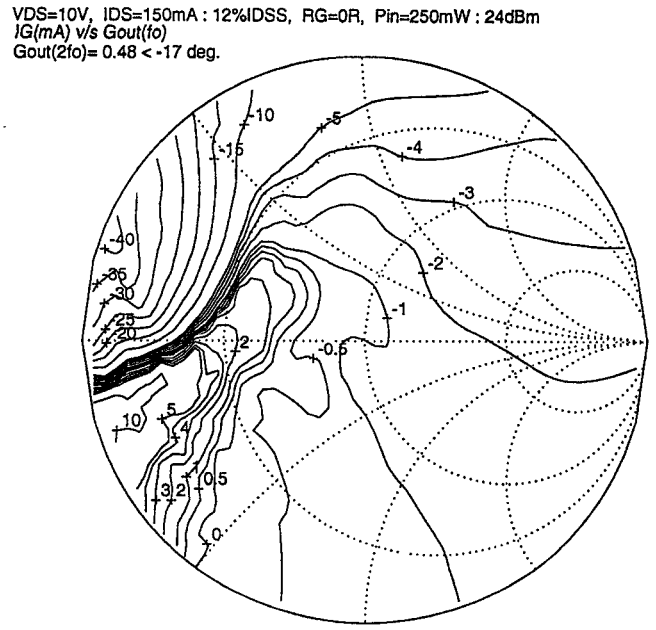


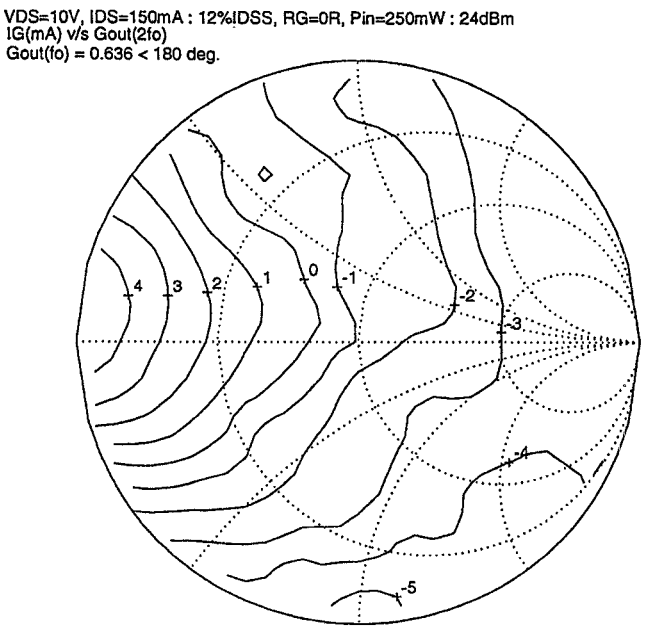
Fig. 3. (a) $P_{\text{out}}(f_0)$ v/s $\Gamma_{\text{out}}(f_0), R_G = 0\ \Omega$. (b) Eff.$(f_0)$ v/s $\Gamma_{\text{out}}(f_0), R_G = 0\ \Omega$. (c) $P_{\text{out}}(f_0)$ v/s $\Gamma_{\text{out}}(f_0), R_G = 270\ \Omega$. (d) Eff.$(f_0)$ v/s $\Gamma_{\text{out}}(f_0), R_G = 270\ \Omega$.

Fig. 3(a) and (b) results reveals that this dependency is particularly pronounced when the output load impedance is near the region of optimum output power or power added efficiency. Moreover, the constant current contours of Fig. 4(a), which correspond to the average values of rf pulsed currents flowing through the gate with a low duty cycle, show that even for an output power not exceeding the 1 dB compression point, the peak values of the rf gate currents can reach very high levels. Fig. 4(b) shows the variation of the average gate current when a compensation resistor $R_G = 270\ \Omega$ is used. The results prove that this value is high enough to substantially reduce the current variations and limits the average gate current between -3 mA and $+2$ mA over the entire Smith chart.

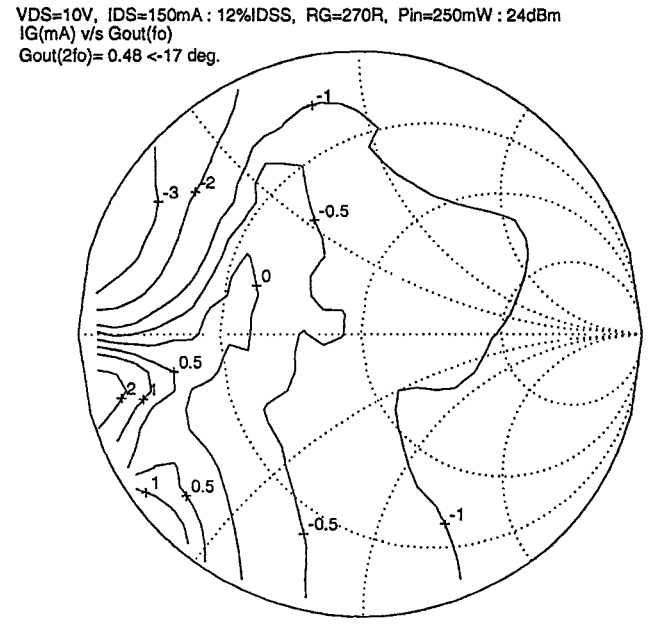
Load-pull measurements on the gate current have also been performed with the same bias and input power condition, but this time as a function of the output impedance at the 3.4 GHz harmonic frequency ($\Gamma_{\text{out}}(2f_0)$), with $\Gamma_{\text{out}}(f_0)$ kept constant. The results for $R_G = 0\ \Omega$ are presented in Fig. 5(a) and show that the dependence of the gate current on $\Gamma_{\text{out}}(2f_0)$ is also quite strong (from -5 mA to $+4$ mA). As shown in Fig. 5(b), a R_G value of 270 Ω is again high enough to significantly reduce the current variations (0 mA to $+1.5$ mA).



(a)

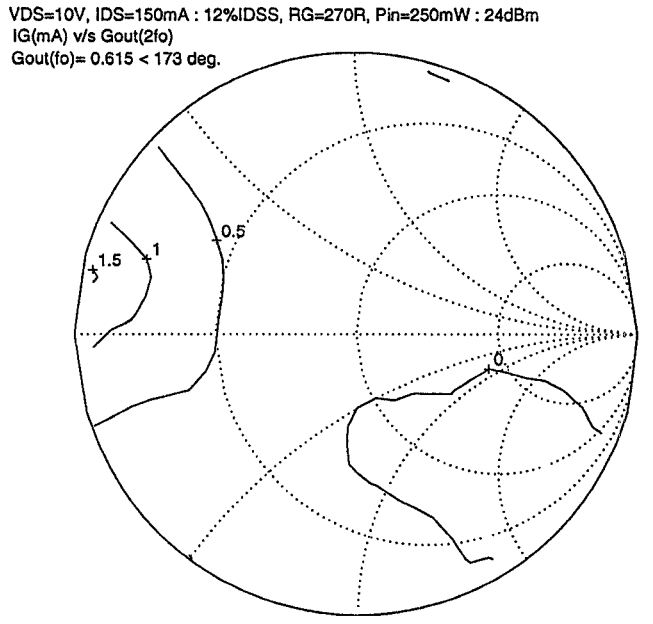


(a)



(b)

Fig. 4. (a) I_G v/s $\Gamma_{\text{out}}(f_0)$, $R_G = 0\,\Omega$. (b) I_G v/s $\Gamma_{\text{out}}(f_0)$, $R_G = 270\,\Omega$.



(b)

Fig. 5. (a) I_G v/s $\Gamma_{\text{out}}(2f_0)$, $R_G = 0\,\Omega$. (b) I_G v/s $\Gamma_{\text{out}}(2f_0)$, $R_G = 270\,\Omega$.

IV. Limitation of Gate Current with Constant Gate Supply Voltage

Thermal runaway conditions [3] may be provoked by a gate resistor when the transistor is biased and when no rf power is applied to its input. Any dc leakage current coming out of the gate [1] will create a voltage drop across R_G (see Fig. 1), moving the bias toward the $V_{GS} = 0$ V condition. Consequently, the drain current is increased and causes a rise in the device temperature. Depending on gate leakage current characteristics of the device as a function of temperature, this process might result in a continuous increase of the power dissipated in the device, which in turn might ultimately lead to the destruction of the device. A large value of R_G increases the sensitivity of the auto-compensation mechanism and thus ensures a better limitation of the gate current over a given range of input power. However, a large R_G value increases the chances that the thermal runaway phenomenon be induced in the absence of input rf power. Therefore a trade-off in the selection of R_G value has to be made.

An experimental approach has been used in order to determine the smallest value of R_G required for the limitation of the gate current within a given dynamic range of the input rf power. Gate current measurements were performed on the

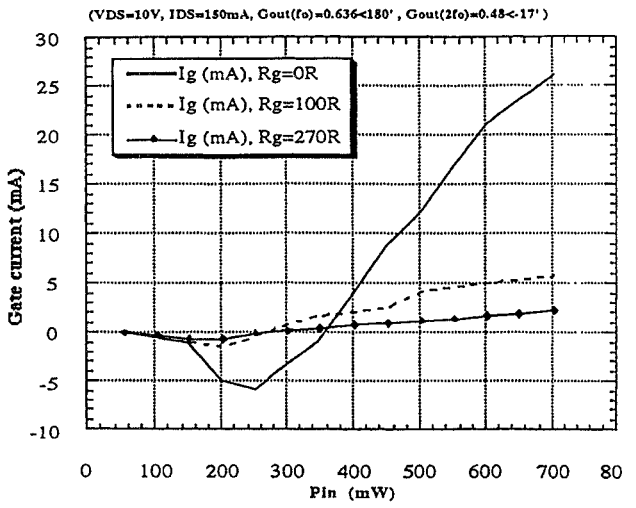


Fig. 6. I_G v/s P_{in} and R_G, in an open loop bias circuit configuration.

GaAs FET as a function of input power and with different values of R_G, while maintaining fixed load and quiescent drain current conditions ($\Gamma_{\text{out}}(f_0) = 0.636\angle 180°, \Gamma_{\text{out}}(2f_0) = 0.48\angle -17°$ and $I_{\text{DS}} = 12\%\ I_{\text{DSS}}$), over a 10 dB dynamic range. Fig. 6 shows the variations of the gate current with R_G values of 0 Ω, 100 Ω, and 270 Ω. The curve corresponding to $R_G = 0\ \Omega$ shows more clearly the predominance of avalanche current at input rf power levels lower than 350 mW and the predominance of forward conduction current at levels above 350 mW for class AB operation mode with this transistor. It can be deduced from these curves that for these load and bias conditions, the maximum values of the average gate current (−2 mA and +4 mA) specified for this transistor require that the input rf power range be limited to two zones: 0 mW to 180 mW and 340 mW to 400 mW for $R_G = 0\ \Omega$. For $R_G \neq 0\ \Omega$, these ranges are continuous: between 0 mW and 500 mW for $R_G = 100\ \Omega$ and between 0 mW and 700 mW for $R_G = 270\ \Omega$. These results are useful for determining the optimum value of R_G required for a given input rf power range. Besides, it has been determined experimentally for this MESFET that in the absence of rf input power and limited heat sinking, the bias point is subject to automatic changes for R_G values of 500 Ω and higher. This indicates that 500 Ω is the minimum R_G value for which the thermal runaway phenomenon may occur and is consequently the upper limit for R_G, in the sense of gate current limitation. From these experimental results it can be deduced that for an input power range of 0 mW to 700 mW, $R_G = 270\ \Omega$ offers a good trade off between gate current limitation and thermal runaway phenomena.

While in general R_G is different from zero, the $R_G = 0\ \Omega$ condition (physical or in the equivalent sense) can be encountered in some applications, such as in MESFET device characterization and in MESFET amplifiers with feedback control on gate biasing. The first application requires that the voltage applied to the gate, V_{GS}, be regulated. In this case, there is no resistor in series with the gate supply voltage regulator. The second one concerns systems requiring that V_{GS} be controlled in a feedback loop as a function of any parameter uncorrelated to the gate current. Linearization methods using dynamic gate biasing with feedback control on V_{GS} [4] are typical examples.

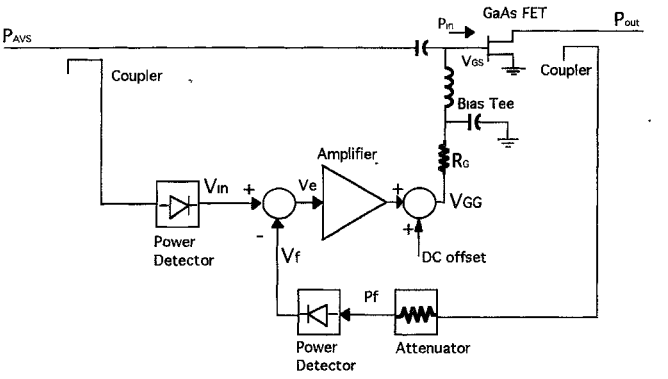


Fig. 7. Typical amplifier structure with feedback controlled V_{GS} for AM-AM linearization.

V. Study of Gate Current Limitation with Feedback Controlled Gate Bias Voltage

When the gate-source bias voltage of a GaAs FET amplifier is controlled in a feedback loop for linearization purposes [4], any voltage drop across the gate resistor R_G, due to an average gate current, will result in an adjustment of V_{GS} through the control loop in order to compensate for this voltage drop. The resulting V_{GS} value is the required voltage to achieve the desired linearization.

Fig. 7 illustrates the typical architecture of a linearized amplifier using feedback control in the gate biasing. Though the GaAs FET's rf power gain is a nonlinear function of V_{GS} and the detector circuits have a nonlinear response, the circuit can be analyzed by approximation using linear control techniques [9] if only small variations of the instantaneous source available power (P_{AVS}) are considered with respect to a given average value. For different P_{AVS} average values, the power detector gain will be different, and the GaAs FET power gain will also vary as a function of the average V_{GS} value. Apart from that, for any P_{AVS} and V_{GS} value, the small signal analysis is valid without any loss of generality. This circuit can be modeled as in Fig. 8, with the following parameter definitions:

K (V/mW)	: combined gain of the input coupler and the input power detector,
G_1 (V/V)	: amplifier voltage gain,
G_2 (V^{-1})	: power conversion factor between P_{in} and P_{out}, and which varies as a function of V_{GS} according to the I_{DS} vs. V_{GS} curve of the GaAs FET,
H_1 (mW/mW)	: combined power gain of the output coupler and the attenuator,
H_2 (V/mW)	: conversion gain of the feedback loop detector,
I_{GS} (A)	: average gate current and
$R_{\text{GS}}(\Omega)$	: equivalent dc load resistance corresponding to $V_{\text{GS}}/I_{\text{GS}}$.

Further simplification of the model leads to the diagram of Fig. 9, where $H = H_1 H_2 G_2 P_{\text{in}}$. The output signal is the

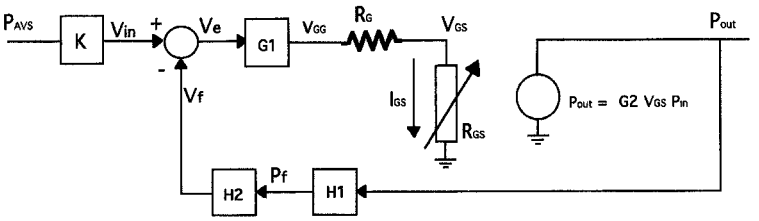


Fig. 8. Detailed linear model of amplifier using feedback linearization method.

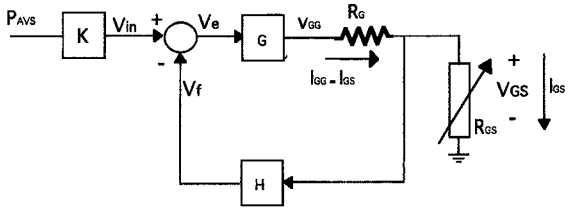


Fig. 9. Simplified model of Fig. 8, with V_{GS} as the output variable.

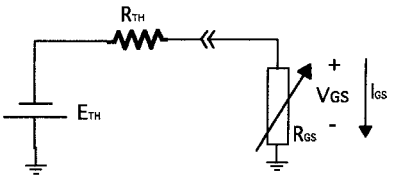


Fig. 10. Equivalent Thevenin circuit of Fig. 9 for a given constant V_{in} value.

average gate current I_{GS} and the input reference is the voltage V_{in} that gives a measure of the input available power. If the feedback control is assumed to be ideal, then for any given V_{in} voltage the proper V_{GSo} voltage required to impose the desired output power will be attained, without any condition on I_{GS}. One consequence of having a nonideal feedback control is that this V_{GSo} voltage may be altered as an average gate current builds up. Such a dependence of V_{GS} on I_{GS} may be modeled by the equivalent Thevenin circuit of Fig. 10. E_{TH} is the V_{GS} voltage attained when there is no gate current and for a specific input available power P_{AVS}. R_{TH} is an equivalent output resistor that converts the increase of the average gate current into a change of the voltage applied to the gate, for the same constant P_{AVS}. Hence, the auto-compensation mechanism for gate current limitation in this feedback architecture depends on the dc equivalent resistance R_{TH} seen from the gate. It is well known that the equivalent output resistance R_{TH} of Fig. 10 may be expressed by

$$R_{TH} = \frac{\Delta V_{GS}}{-\Delta I_{GS}}, \text{ for a given } P_{AVS}. \tag{1}$$

Applying (1) to the circuit of Fig. 9, R_{TH} can be expressed as

$$R_{TH} = \frac{R_G}{1 + GH} \tag{2}$$

and E_{TH} can be expressed as

$$E_{TH} = \frac{G}{1 + GH} V_{in}. \tag{3}$$

According to (2), even if a series compensation resistor R_G is physically present, the equivalent Thevenin resistor seen from the gate may be close to zero if the loop gain GH is high enough. Therefore, depending on the loop gain and the R_G value used, it is expected that the gate current variations in amplifiers using feedback controlled V_{GS} might exceed the safety limits and thus might present long term reliability problems. Furthermore, it is believed that an evaluation of the values of the loop gain and R_G should enable the designer to use (2) and gate current characterization curves similar to those of Fig. 6 (which have been measured in an open loop biasing circuit as in Fig. 1) to estimate the gate current in a closed loop biasing circuit as in Fig. 7.

VI. Experimental Data on Gate Current Limitation with Feedback Controlled Gate Bias Voltage

A linearized amplifier identical to the circuit of Fig. 7 has been used for these measurements. The GaAs FET used is the same as what has been used for the measurements of Fig. 6. The measured loop gain GH was equal to 45. Gate current measurements have been performed as a function of the input power and with different RG values (0 Ω and 270 Ω). The results are shown in Fig. 11. These results indicate that in this bias configuration, the current variations for both R_G values are very similar over the input power range of 0 mW to 350 mW, whereas in the open loop configuration the current variations for the same R_G values (0 Ω and 270 Ω) were very different (see Fig. 6). This can be explained with the help of (2). The loop gain GH = 45 implies that the equivalent Thevenin resistor seen from the gate is 5.9 Ω when R_G = 270 Ω. Therefore the behavior of the gate current in this case is inevitably similar to the case R_G = 0 Ω. Besides, it has been verified experimentally that the gate current behavior in these two cases (R_G = 0 Ω and R_G = 6.8 Ω) are as similar in the open loop bias configuration. Thus these results indicate that (2) can be used for an approximate prediction of the average current in the closed loop bias configuration, if the current behavior has been characterized in the open loop configuration. Moreover, these results show that the widely used method of limiting the gate current with resistor R_G may be ineffective when the gate is biased with a feedback loop. In the case of linearized SSPA's with the feedback method, even if a gate resistor is physically present, the average gate current variations may exceed the safety limits and hence may present long term reliability problems.

The current curve for R_G = 270 Ω in Fig. 11 indicates that the current limitation is more efficient than in the case R_G = 0 Ω for an input power higher than 350 mW. During

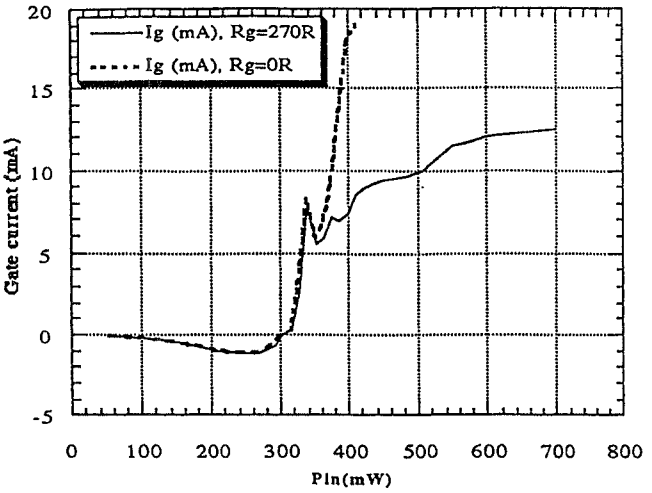


Fig. 11. I_G v/s P_{in} and R_G, in a closed loop bias circuit configuration.

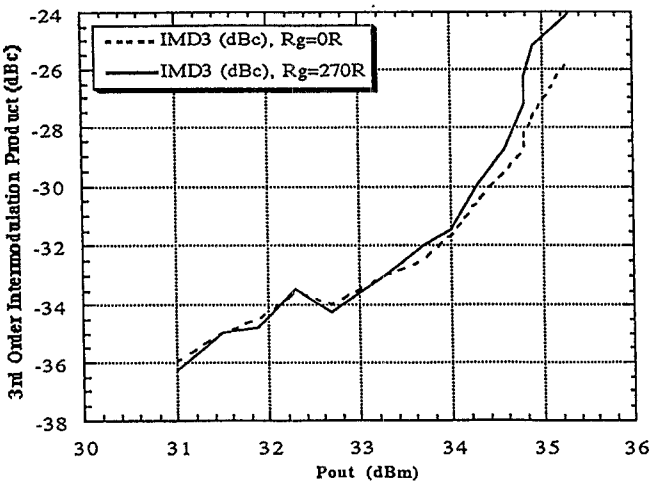


Fig. 12. Effects of gate current limitation on intermodulation levels.

the experiments, it has been verified that this difference is not due to any current or voltage saturation in the bias circuit. The difference can be explained by the gain compression of the GaAs FET which implies a smaller loop gain, and thus a higher equivalent Thevenin resistor seen from the gate, allowing a more efficient current limitation.

A comparison based on Figs. 6 and 11 reveals that the gate current behavior as a function of input power with $R_G = 0\ \Omega$ are not identical. Though the equivalent Thevenin resistor is the same in both configurations when $R_G = 0\ \Omega$, the average V_{GS} voltages as a function of the input power are different. It is kept constant in the open loop configuration and varies in the closed loop configuration.

VII. Measurements of Gate Current Limitation Effects on Third Order Intermodulation Levels

Using a two tone intermodulation test with a frequency spacing of 5 KHz, the effects of gate current limitation on the intermodulation levels were measured on the linearized amplifier illustrated in Fig. 7. The results presented in Fig. 12 show the third order intermodulation levels with $R_G = 0\ \Omega$ and $R_G = 270\ \Omega$. A slight difference can be observed for output power levels above the output 1 dB compression point. For these power levels, the intermodulation product is slightly lower in the case where $R_G = 0\ \Omega$. In this case the dynamic biasing of V_{GS} is independent of the average gate current. However, in the case where $R_G = 270\ \Omega$, the dynamic biasing of V_{GS} becomes more and more perturbed by the gate current when the output power is above the compression point, since this causes the loop gain to decrease. As a result, the linearization process becomes less efficient.

VIII. Conclusion

An experimental investigation of the effects of gate current on rf performances of a power GaAs FET has been performed. It has been shown that the output power and power added efficiency performances are not altered by the gate current limitation. However a slight change in the optimum load conditions has been observed. For the first time, load-pull measurements on gate current have been presented and show a strong dependence of the gate current on the output load at the fundamental and second harmonic frequencies. An experimental approach has been used to select the value of the gate resistor that offers the best trade-off between current limitation and thermal runaway conditions. The gate current limitation mechanism within the typical feedback architecture used for amplifier linearization has been discussed. It has been shown with the help of experimental results that the widely used method of limiting the gate current with a series resistor in the dc path start to be effective only above compression levels, when the gate is biased with a feedback loop. This may lead to average gate current variations exceeding the safety limits of the GaAs FET and hence may present long term reliability problems. Intermodulation measurements have been performed on a feedback linearized amplifier. Experimental results showing the gate current limitation effects on intermodulation product levels have been presented, and a slight improvement has been observed in the case where the feedback mechanism is not perturbed by the average gate current.

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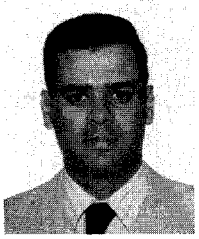

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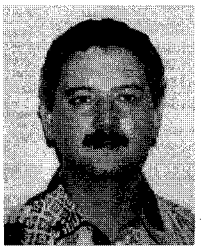

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